

**APPARATUS AND METHOD FOR PERFORMING STATIC TIMING
ANALYSIS OF AN INTEGRATED CIRCUIT DESIGN**

ABSTRACT OF THE DISCLOSURE

5 An apparatus and method perform static timing analysis on an integrated circuit
design. Certain pessimistic assumptions regarding slack when data launch and clock test
signals are on opposite edges and derived from common logic blocks are improved by
allowing the designer to identify common logic blocks, to compute the difference between
maximum and minimum delays in the common logic blocks, and to improve the slack
using this computed difference and a correction factor, thereby accounting for excessive
10 pessimism in the static timing analysis that results from the common logic blocks. The
apparatus and method give credit for slack in common blocks automatically, thereby
allowing a large number of pessimistic slack values to be automatically corrected and
reducing the workload of an integrated circuit designer in addressing the timing problems
in an integrated circuit design.